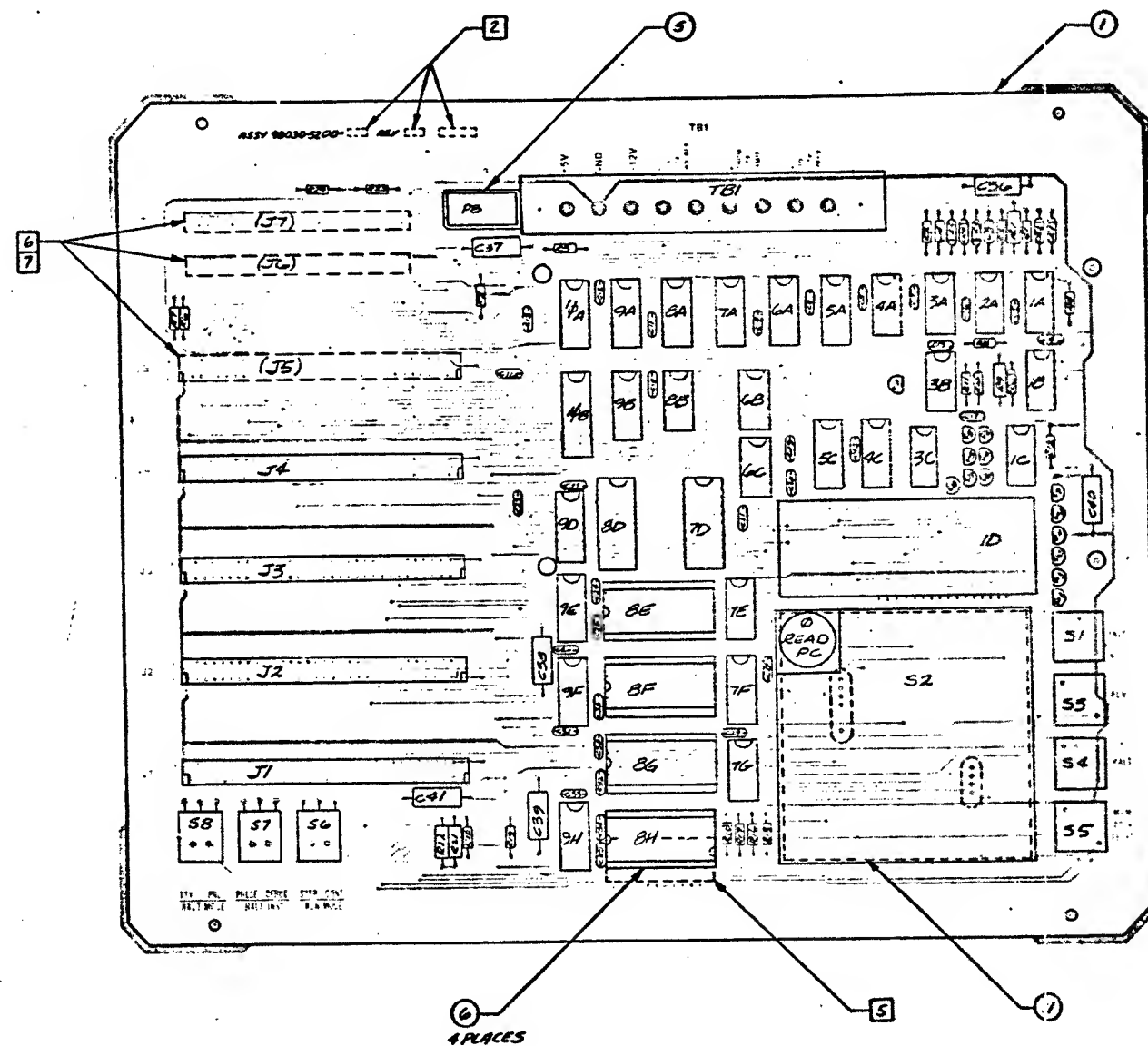


REVISIONS			
APPROVED	DATE	CHK NUMBER	REV
<i>Long Glt</i>	6-10-71	PROD. RB. 3157-0405	A
<i>Long Glt</i>	7/1/71	DCN IMP-2678	B
<i>Long Glt</i>	7-22-71	DCN IMP-2727	C
<i>Long Glt</i>	7-22-71	DCN IMP-2492	D

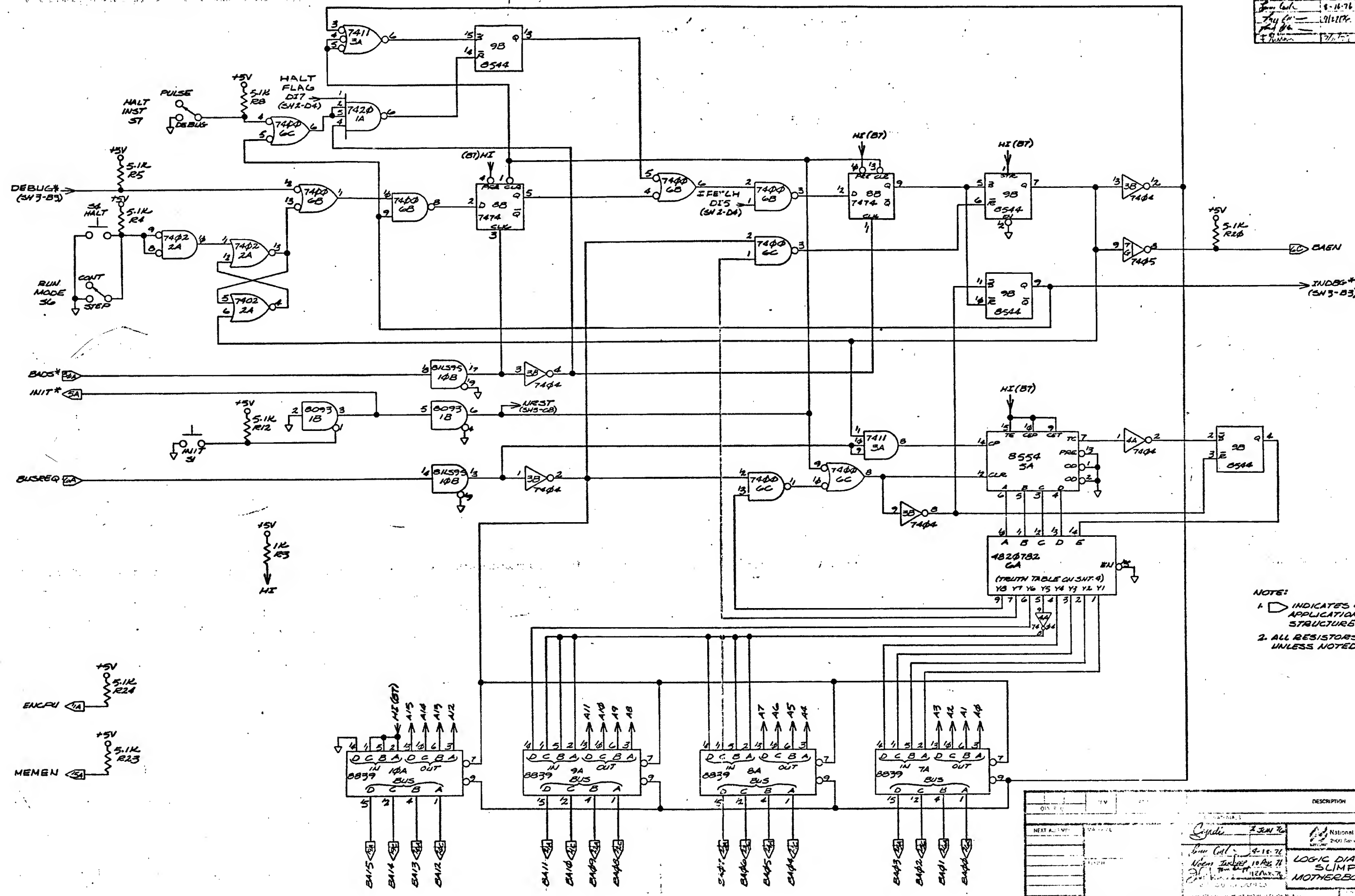


NOTE - UNLESS OTHERWISE SPECIFIED:

1. FRONT SIDE CIRCUITRY SHOWN SHADED FOR CLARITY
2. MARK APPLICABLE DASH NO., REV LEVEL AND S/N J2 -18 HIGH CHARACTERS APPROX. AS SHOWN
3. FOR LOGIC DIAGRAM SEE 870305200
4. LOCATION NO/REF DES SHOWN FOR REF
5. HOLE PATTERN (BU) FOR FUTURE OPTION
6. J5, J6 & J7, ARE OPTIONAL (CUSTOMER INSTALLS)
7. HOLES FOR J5, J6, J7 (164 HOLES) ARE TO BE FREE OF SOLDER

[illegible]

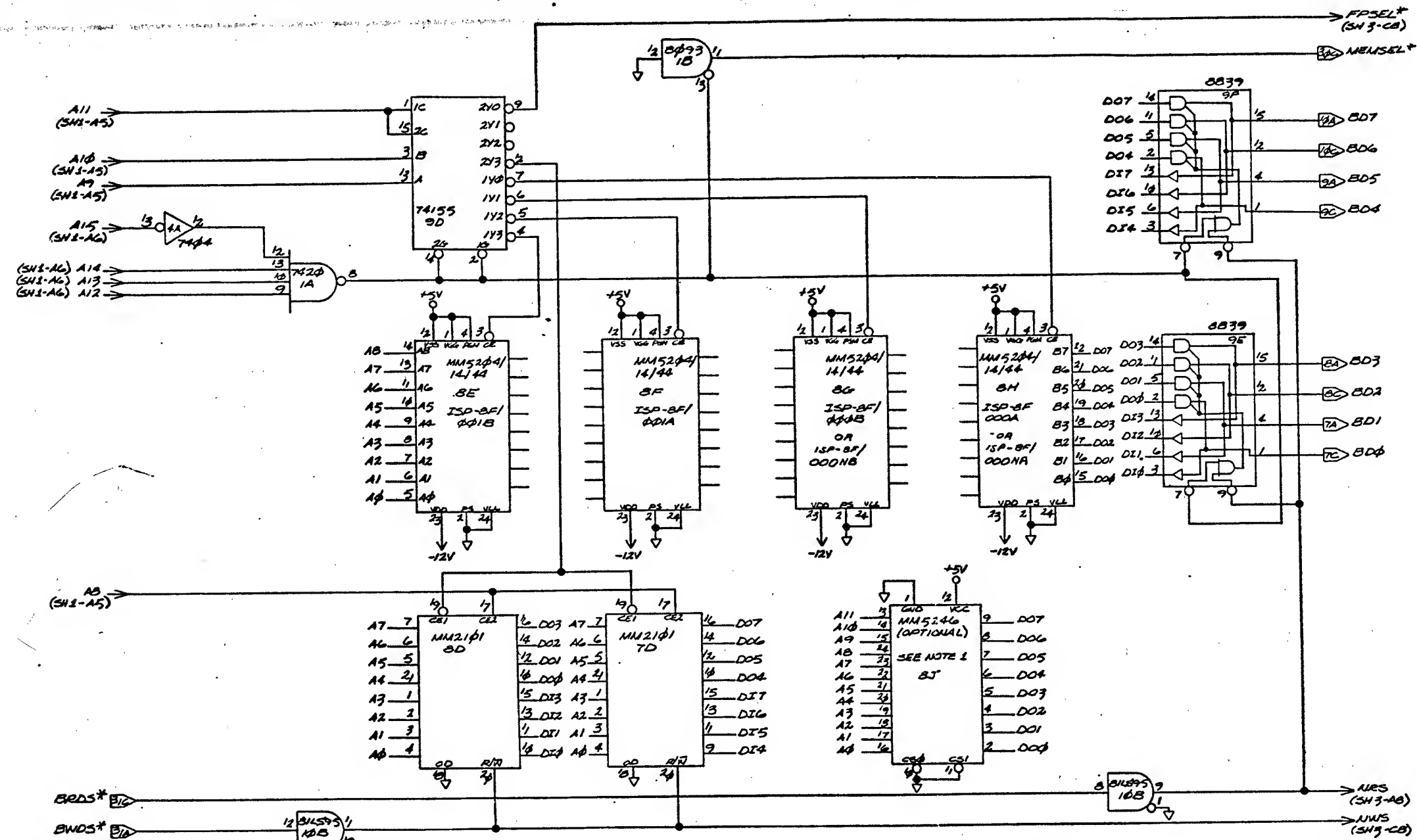
APPROVED	DATE	CLN. NUMBER	REV.
John Cull	8-18-76	PROD. REL. 203-0409	A
Paul G.	9/1/76	DCN IMP-2678	B
Paul G.	9/1/76	DCN IMP-2787	C
Paul G.	9/1/76	DCN IMP-2792	D



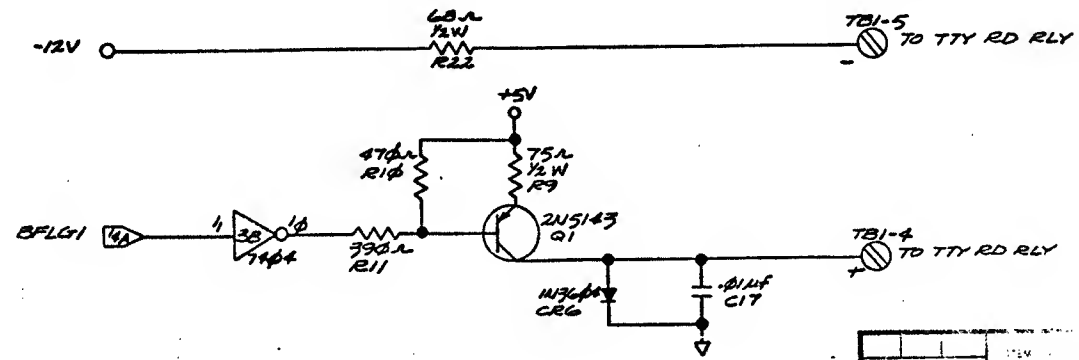
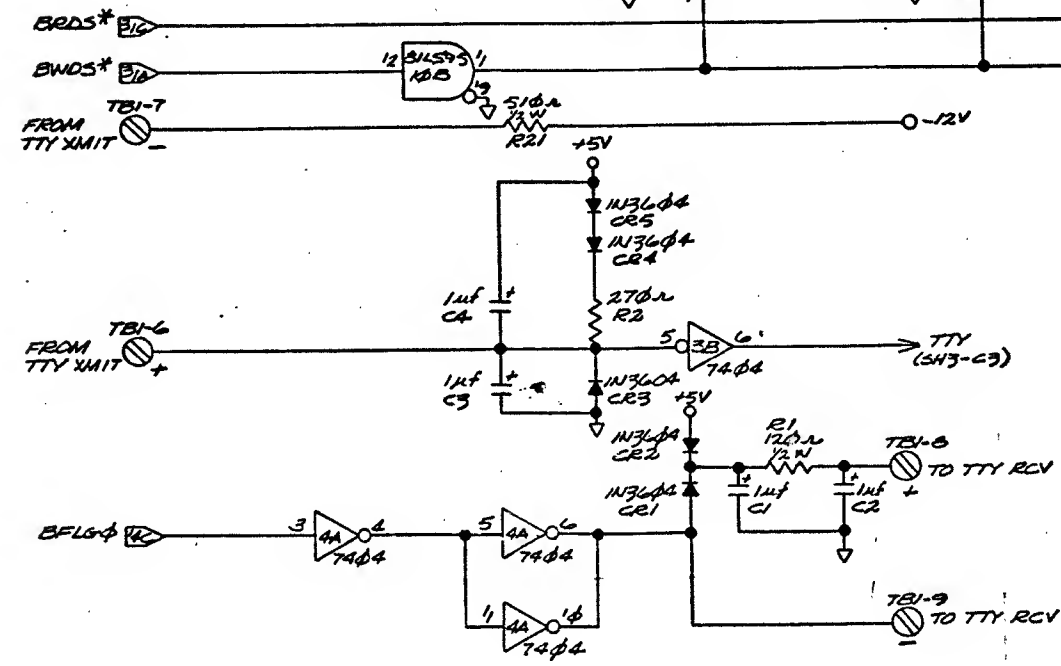
NOTE:  
 1. INDICATES CONNECTION TO APPLICATION CARD BUS STRUCTURE. SEE SHEET 4.  
 2. ALL RESISTORS 1/4 W, 5% UNLESS NOTED.

DESCRIPTION	
LOGIC DIAGRAM - SLIMP LCD's MOTHERBOARD LOGIC (EUKO LARD)	
U 870305200	D
NOTE: 1 4	

REVISIONS		
APPROVED	DATE	BY
		SEE SH1



NOTE:  
 1. WHEN MM5246 2K X 8 ROM IS USED, ROM FROM BE - BH ARE NOT USED ON THE BOARD.  
 2. A0 - AB AND D00 - D07 ARE TIED TOGETHER RESPECTIVELY ON BE, BF, BG, AND BH.



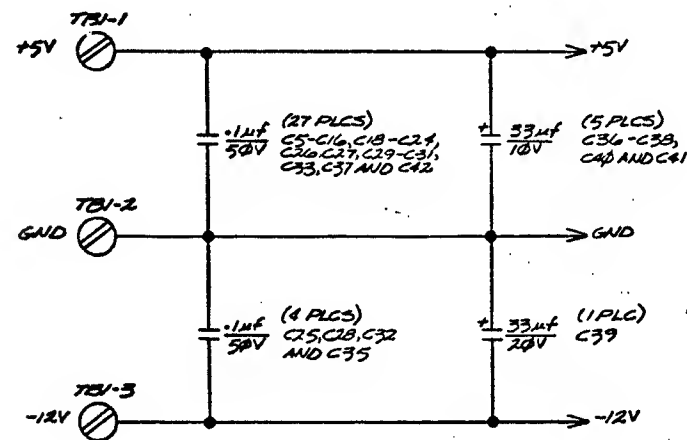
QTY	ITEM	DESCRIPTION
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1	74153	74153
1	74152	74152
1	74151	74151
1	74150	74150
1	74149	74149
1	74148	74148
1	74147	74147
1	74146	74146
1	74145	74145
1	74144	74144
1	74143	74143
1	74142	74142
1	74141	74141
1	74140	74140
1	74139	74139
1	74138	74138
1	74137	74137
1	74136	74136
1	74135	74135
1	74134	74134
1	74133	74133
1	74132	74132
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1	74130	74130
1	74129	74129
1	74128	74128
1	74127	74127
1	74126	74126
1	74125	74125
1	74124	74124
1	74123	74123
1	74122	74122
1	74121	74121
1	74120	74120
1	74119	74119
1	74118	74118
1	74117	74117
1	74116	74116
1	74115	74115
1	74114	74114
1	74113	74113
1	74112	74112
1	74111	74111
1	74110	74110
1	74109	74109
1	74108	74108
1	74107	74107
1	74106	74106
1	74105	74105
1	74104	74104
1	74103	74103
1	74102	74102
1	74101	74101
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1	74015	74015
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1	74008	74008
1	74007	74007
1	74006	74006
1	74005	74005
1	74004	74004
1	74003	74003
1	74002	74002
1	74001	74001
1	74000	74000



TRUTH TABLE OF ROM LOCATED AT 4820782											
E	D	C	B	A	Y <sub>8</sub>	Y <sub>7</sub>	Y <sub>6</sub>	Y <sub>5</sub>	Y <sub>4</sub>	Y <sub>3</sub>	Y <sub>2</sub>
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0	0	0	0	1	0	0	1	1	0	0	0
0	0	0	1	0	0	0	1	1	0	0	0
0	0	0	1	1	0	0	0	0	1	1	0
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0	0	1	0	1	0	0	1	1	0	0	1
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0	1	0	0	0	0	0	1	1	0	0	0
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1	1	1	1	1	0	0	0	0	1	0	1

PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME
1A	+5V	1C	+5V
2A	+15V	2C	+15V
3A	-12V	3C	-12V
4A	GND	4C	GND
5A	INIT*	5C	MEMRDY
6A	BUSREQ	6C	BAEN
7A	BDI	7C	BD2
8A	BD3	8C	BD2
9A	BD5	9C	BD4
10A	BD7	10C	BD6
11A	ENCPU	11C	RUN
12A	BSENSE	12C	ASENSE
13A	BSOUT	13C	BSIN
14A	BFLG1	14C	BFLG2
15A	MEMEN	15C	BFLG2
16A	GND	16C	GND
17A	READ	17C	DELAY
18A	HALT	18C	IFETCH
19A	BA15	19C	BA14
20A	BA13	20C	BA12
21A	BA11	21C	BA10
22A	BA09	22C	BA08
23A	BA07	23C	BA06
24A	BA05	24C	BA04
25A	BA03	25C	BA02
26A	BA01	26C	BA00
27A	USER 4	27C	USER 3
28A	ENI*	28C	ENI
29A	ROMSEL	29C	RIMSEL
30A	BADS*	30C	MEMSEL*
31A	BWDS*	31C	BRDS*
32A	GND	32C	GND

PIN CONNECTIONS, 5 PLACES, J1 THROUGH J5



PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME
2	MEMRDY	1	GND
4	BAEN	3	GND
6	BDI	5	GND
8	BD2	7	GND
10	BD4	9	GND
12	BD6	11	GND
14	RUN	13	GND
16	ASENSE	15	GND
18	BSIN	17	GND
20	BFLG1	19	GND
22	BFLG2	21	GND
24	READ	23	GND
26	HALT	25	GND
28	BA15	27	GND
30	BA13	29	GND
32	BA11	31	GND
34	BA09	33	GND
36	BA07	35	GND
38	BA05	37	GND
40	BA03	39	GND
42	BA01	41	GND
44	USER 4	43	GND
46		45	GND
48	BADS*	47	GND
50	BWDS*	49	GND

PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME
2	INIT*	1	GND
4	BUSREQ	3	GND
6	BDI	5	GND
8	BD3	7	GND
10	BD5	9	GND
12	BD7	11	GND
14	ENCPU	13	GND
16	BSENSE	15	GND
18	BSOUT	17	GND
20	BFLG1	19	GND
22	MEMEN	21	GND
24	DELAY	23	GND
26	IFETCH	25	GND
28	BA14	27	GND
30	BA12	29	GND
32	BA10	31	GND
34	BA08	33	GND
36	BA06	35	GND
38	BA04	37	GND
40	BA02	39	GND
42	BA00	41	GND
44	USER 3	43	GND
46		45	GND
48	MEMSEL*	47	GND
50	BRDS*	49	GND

REVISIONS	
APPROVED	DATE
SEE SHIT 1	

CABLE CONNECTOR J6	
PIN NO.	SIGNAL NAME
2	MEMRDY
4	BAEN
6	BDI
8	BD2
10	BD4
12	BD6
14	RUN
16	ASENSE
18	BSIN
20	BFLG1
22	BFLG2
24	READ
26	HALT
28	BA15
30	BA13
32	BA11
34	BA09
36	BA07
38	BA05
40	BA03
42	BA01
44	USER 4
46	
48	BADS*
50	BWDS*

CABLE CONNECTOR J7	
PIN NO.	SIGNAL NAME
2	INIT*
4	BUSREQ
6	BDI
8	BD3
10	BD5
12	BD7
14	ENCPU
16	BSENSE
18	BSOUT
20	BFLG1
22	MEMEN
24	DELAY
26	IFETCH
28	BA14
30	BA12
32	BA10
34	BA08
36	BA06
38	BA04
40	BA02
42	BA00
44	USER 3
46	
48	MEMSEL*
50	BRDS*

DESCRIPTION	
QTY	DESCRIPTION
1	LOGIC DIAGRAM - SLIMP LCDS MOTHERBOARD LOGIC (EURO CARD)
1	810305200
1	NONE